# Voice coil amplifier[[1]](#footnote-1)

## 1.0 Overview

A block diagram of the voice coil amplifier is show in Figure 1 over-leaf. The main features of this amplifier are;

1. All digital input control using a CAT 6 cable.
2. Three 16-bit DAC’s to control the output current from the transconductance amplifiers to the voice coils.
3. One, 4 channel, 16-bit ADC.
4. Two channels of the ADC have amplified inputs. The gains of these two amplifiers can be manually set using a four switch array on the amplifier box. All four ADC channels can also be set to two input ranges (5 V and 10 V) either unipolar or bipolar (0 – 5 V, 0 – 10 V, ±5 V or ±10 V).
5. Information and controls of both ADC and DAC are communicated using four SPI buses.
6. Programs for data acquisition using NI myRIO hardware will be supplied.
7. A three throw switch is used to turn off the amplifiers. Amplifiers should only be switched on when the DAC’s have been set to zero volts.
8. A ±15 V external power supply and LED on the RJ45 connector indicating ‘power on’ when illuminated.
9. Three transconductance amplifiers to supply currents to the voice coil actuators controlled by the DAC’s.
10. Three sense outputs from 2.2 Ω power resistors to monitor current through the voice coils.

Each of these are discussed in individual sections. Photographs showing front, back and isometric views of the amplifier ae shown in Figure 2. A total of ten amplifiers have been made and these are identified by the upper case letters A through J.

## 2.0 All digital control

An RJ45 connector is available on the front panel of the amplifier. This is designed to receive a CAT 6 shielded cable connector. The other end of the supplied cable is broken out to individual wires for connecting to the terminal strip connector of the myRIO.

Four of the wires are used to select the channels and input gains (using MOSI 1) and read the voltage values from the ADC (using MISO 1). Serial transfer for the both the ADC and all three DAC’s is controlled by chip select (CS) and clock 1 (CLK 1). Datasheets for the LTC1859CG ADC can be obtained at;

<https://www.analog.com/media/en/technical-documentation/data-sheets/185789fb.pdf>

The other four wires are used to control the three AD420 DAC chips. This can accept a faster clock speed than the ADC and is provided with a separate clock (CLK2). All three DAC’s can be controlled with three MOSI data lines. Data sheets for the AD420 can be obtained at;

<https://www.analog.com/media/en/technical-documentation/data-sheets/AD420.pdf>

Nine digital wires from a CAT6 ethernet cable are used to transfer binary control signals from the myRIO to the amplifier. Bare wires with pin connector are used at one end of the CAT6 cable while the other end plugs into the amplifier using and RJ45 connector.

The function of the digital lines is shown in Table 1.

|  |
| --- |
|  |
| Figure : Schematic diagram of wires in a CAT6 cable (left), cable supplied for connecting the amplifier to the myRIO. |

Table : Table showing wires of the CAT6 cable and associated function for digital amplifier control.

|  |  |  |
| --- | --- | --- |
| **Cat6 wire #** | **Wire color** | **myRIO function** |
| 1 | o/ | MISO1 |
| 2 | O | MOSI1 |
| 3 | g/ | CLK1 |
| 4 | B | CS |
| 5 | b/ | CLK2 |
| 6 | G | MOSI2 |
| 7 | br/ | MOSI3 |
| 8 | Br | MOSI4 |
| GND | Silver | GND |

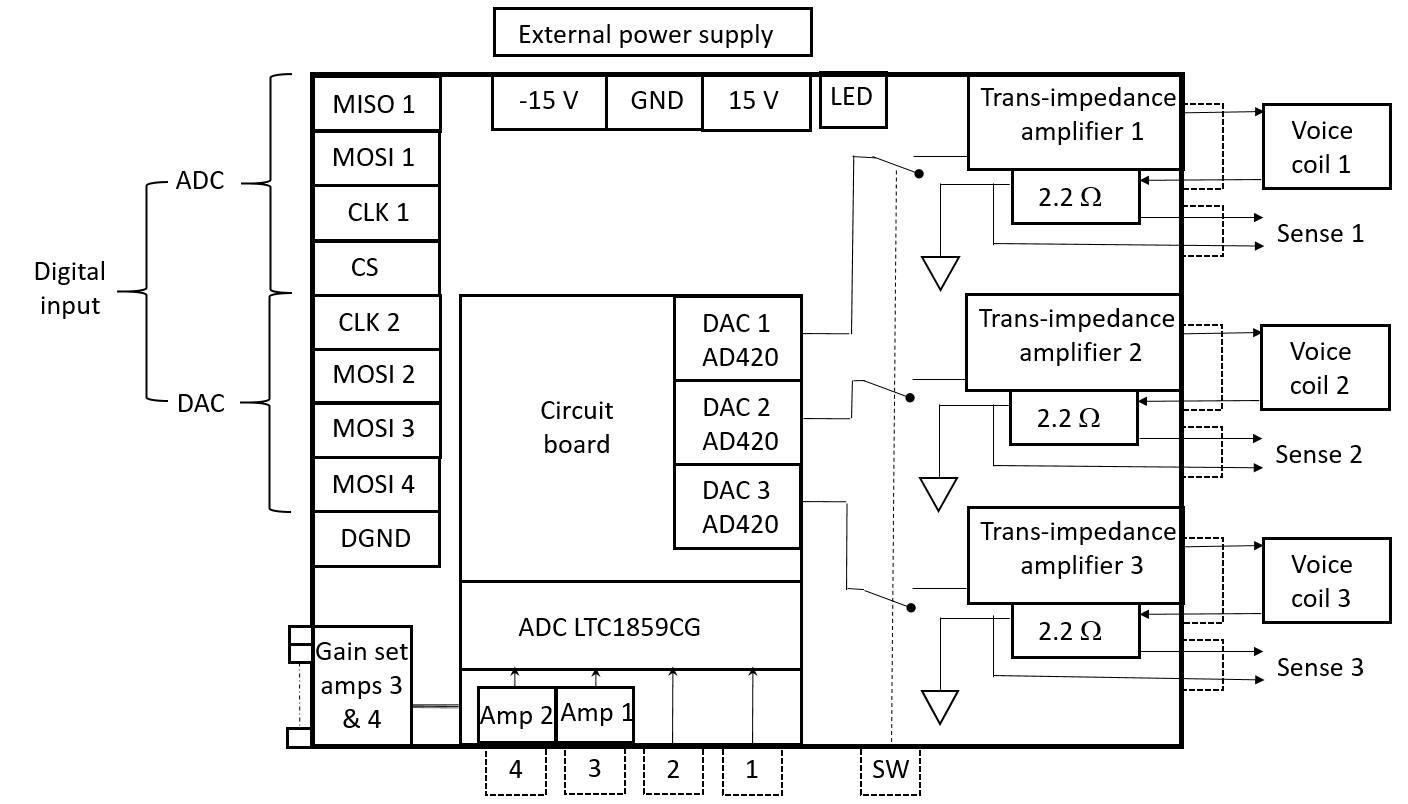


Figure : Block diagram of the voice coil amplifier for the ASPE student challenge.

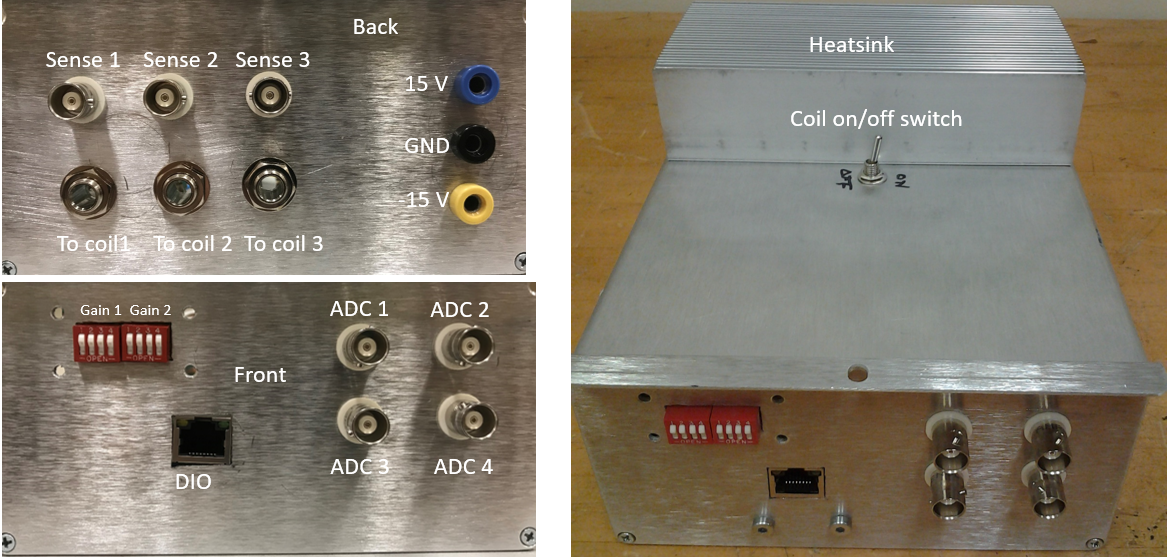


Figure : Photograph of the amplifier, back panel (upper left), front panel (lower left), osimetric view (right).

## 3.0 Single channel 16 bit DAC

The 16 bit DACs are designed to provide ±10 V to the inputs of the transconductance amplifiers that, in turn, have a gain of 0.1016 A⋅V-1. Therefore the DACs can be used to control a maximum current of ±1.016 A to the voice coils. The output from each DAC is filtered using a 2nd order Salen-Key low pass filter with a cut-off at 10 kHz. Note that power supplies can only provide a maximum of 3 A. Consequently, the magnitude sum of currents must always be below this limit.

## 4.0 Four channel 16-bit ADC

The analogue to digital converter has four differential inputs programmable to accept input ranges of 0 – 5 V, 0 – 10 V, ±5 V, and ±10 V. Selecting the channels to be read and input voltage range for each channel is achieved using the supplied myRIO software, see section 8.0. Standard BNC connectors on the front panel of the amplifier are used to connect voltage signals to the ADC.

## 5.0 Selecting input gains on two ADC channels

Two of the four ADC channels (channels 3 and 4) receive inputs via an instrumentation amplifier (INA 821, see link below). Amplifier gain is achieved by selecting a suitable feedback resistance using a manual selection switch, see Figure 4. Table 2 lists the values of four resistors that provide the capability of selecting sixteen gain values listed in Table 3. For a total value of resistance (expressed in kΩ) the gain, , is computed from



Because these gains are based on nominal resistance values, five different gain settings (1, 1.97, 2.5, and 4.3) will be calibrated prior to the competition and entered into Table 3.



Figure : Circuit diagram showing the selection of resistance values for the instrumentation amplifier.

Table : Values of resistors (kΩ) for selecting gain on the instrumentation amplifiers feeding two ADC channels.

|  |  |  |  |
| --- | --- | --- | --- |
| **R1** | **R2** | **R3** | **R4** |
| 6.2 | 15 | 33 | 51 |

Table : Instrumentation amplifier gains as a function of the four, manually selected, switch settings.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Logic settings** | |  |  |  |  |  |
| **S1** | **S2** | **S3** | **S4** |  | **Gain** | **Calibrated gain** |
| 0 | 0 | 0 | 0 | 1E+15 | 1.0000 |  |
| 1 | 0 | 0 | 0 | 6.2 | 8.9677 |  |
| 0 | 1 | 0 | 0 | 15 | 4.2933 |  |
| 1 | 1 | 0 | 0 | 4.39 | 12.2611 |  |
| 0 | 0 | 1 | 0 | 33 | 2.4970 |  |
| 1 | 0 | 1 | 0 | 5.22 | 10.4647 |  |
| 0 | 1 | 1 | 0 | 10.3 | 5.7903 |  |
| 1 | 1 | 1 | 0 | 3.87 | 13.7580 |  |
| 0 | 0 | 0 | 1 | 51 | 1.9686 |  |
| 1 | 0 | 0 | 1 | 5.53 | 9.9364 |  |
| 0 | 1 | 0 | 1 | 11.6 | 5.2620 |  |
| 1 | 1 | 0 | 1 | 4.04 | 13.2297 |  |
| 0 | 0 | 1 | 1 | 20.0 | 3.4656 |  |
| 1 | 0 | 1 | 1 | 4.73 | 11.4333 |  |
| 0 | 1 | 1 | 1 | 8.58 | 6.7589 |  |
| 1 | 1 | 1 | 1 | 3.60 | 14.7267 |  |

Datasheet for the instrumentation amplifier can be obtained at;

<http://www.ti.com/lit/ds/symlink/ina821.pdf>

## 6.0 Transconductance amplifier switch

Because the amplifiers are potentially capable of delivering up to 2 A, there is a possibility of delivering upwards of 20 W to a single coil that can result in high temperatures in the winding and possible damage.

To prevent damage to either the coils or amplifiers, a three pole double throw (TPDT) switch is available on the front panel of the amplifier. This should always be set to ‘off’ when the coils are not being used. In the ‘off’ state, the output of the amplifier is disconnected from the coils.

Never disconnect coils with the ‘Coils’ switch set to ‘on’.

### 6.1 Starting procedure

Step1

Prior to turning on the amplifier, make sure that all necessary coils are connected. Unconnected channels will not be damaged under any circumstance.

Step 2

Plug in the power cable and check that the LED on the front panel as well as the LED on the RJ45 connector are illuminated.

Step 3

Run the hardware interface program and set all coils to zero output current.

Step 4

Flip the ‘Coils’ switch from ‘off’ to ‘on’.

### 6.2 Shut down procedure

Step 1

Run the hardware interface program and set all coils to zero output current.

Step 2

Flip the ‘coils’ switch from ‘on’ to ‘off’.

## 7.0 Transconductance amplifiers

As stated in section 3.0, there are three transconductance amplifiers each having a gain of 0.1 A⋅V-1. Detailed circuit diagrams and relevant formulas are provided in the hardware file. Current from the amplifiers is fed through a 2.2 Ω, 50 W metal film resistor that feeds directly to ground. The voltage across this sense resistor is connected to a BNC socket accessible on the outside rear panel of the amplifier. Each resistor has been measured at room temperature with an estimated uncertainty (k = 2) of 1 mΩ and values for the specific amplifiers are provided in Table 4.

Table : Values of the sense resistors for the three output channels (values for the last five amplifiers have yet to be measured).

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Amplifier/Channel | A | B | C | D | E | F | G | H |
| 1 | 2.1970 | 2.2025 | 2.1978 | 2.1979 | 2.2023 | 2.18105 | 2.19861 | 2.19855 |
| 2 | 2.1989 | 2.2180 | 2.1975 | 2.1990 | 2.20065 | 2.19815 | 2.19846 |  |
| 3 | 2.1968 | 2.1979 | 2.1968 | 2.1972 | 2.1943 | 2.19743 | 2.18231 |  |

Datasheets for these resistors are at;

<https://www.digikey.com/product-detail/en/TR35JBL2R20/TR35JBL2R20-ND/1646137/?itemSeq=298831150>

## 8.0 Labview user interface

An example Labview™ project (‘ASPEStudentChallenge2019.lvproj’) providing an interfaces to control the amplifier is supplied. The project contains two programs. FPGA\_SPI.vi connects to digital pins on the ‘A’ connector of the myRIO. Wiring of the CAT6 wires to this connector is given in Table 5. A cable with plug-in for the myRIO connector will be supplied with the amplifier

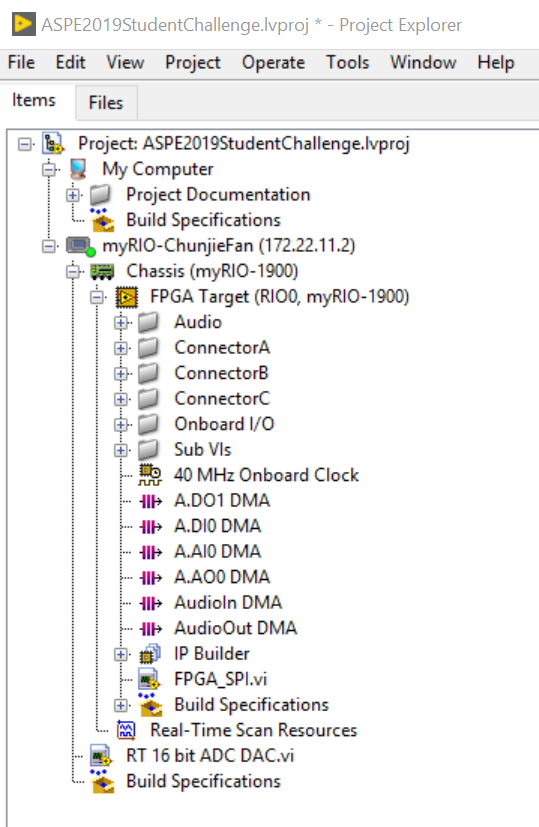
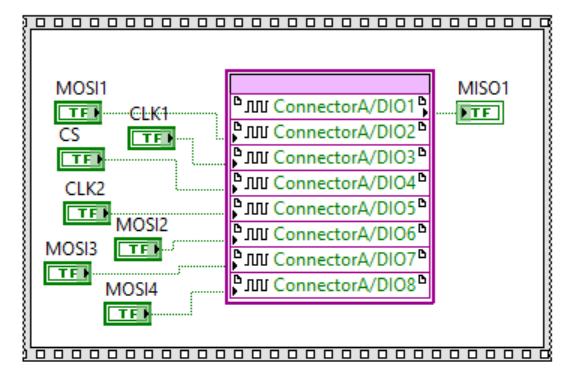
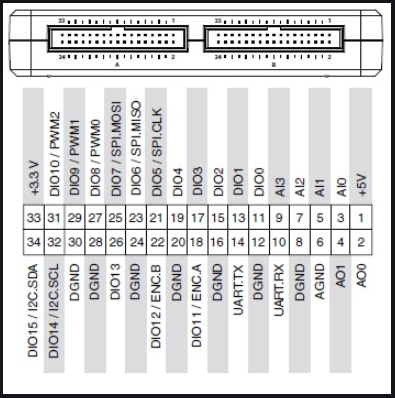


Figure : Project explorer for the amplifier control software (red circles indicate the two control programs).

Table : Physical connections of CAT6 wires to connector 'A' of the myRIO and FPGA block diagram for SPI interface and pin layout for the A and B connectors of the myRIO.

|  |  |  |  |
| --- | --- | --- | --- |
| **Connector A** | **Wire color** | **myRIO function** | **Connector A pin #** |
| DIO1 | o/ | MISO1 | 13 |
| DIO2 | O | MOSI1 | 15 |
| DIO3 | g/ | CLK1 | 17 |
| DIO4 | B | CS | 19 |
| DIO5 | b/ | CLK2 | 21 |
| DIO6 | G | MOSI2 | 23 |
| DIO7 | br/ | MOSI3 | 25 |
| DIO8 | Br | MOSI4 | 27 |
| GND | Silver | GND | 12 |

The GUI of the main real time program (‘RT 16 bit ADC DAC.vi’) is shown in Figure 6. Dependent upon whether the button is on or off, this program is capable of sending either a sinusoidal (button ‘off’) or DC (button ‘on’) voltage from all three DAC’s that provide input to all three transconductance amplifiers. Because the sensitivity of the transconductance amplifiers is 0.1 A⋅V-1, at the maximum output of 10 V, a current of 1 A will be passing through the voice coils.

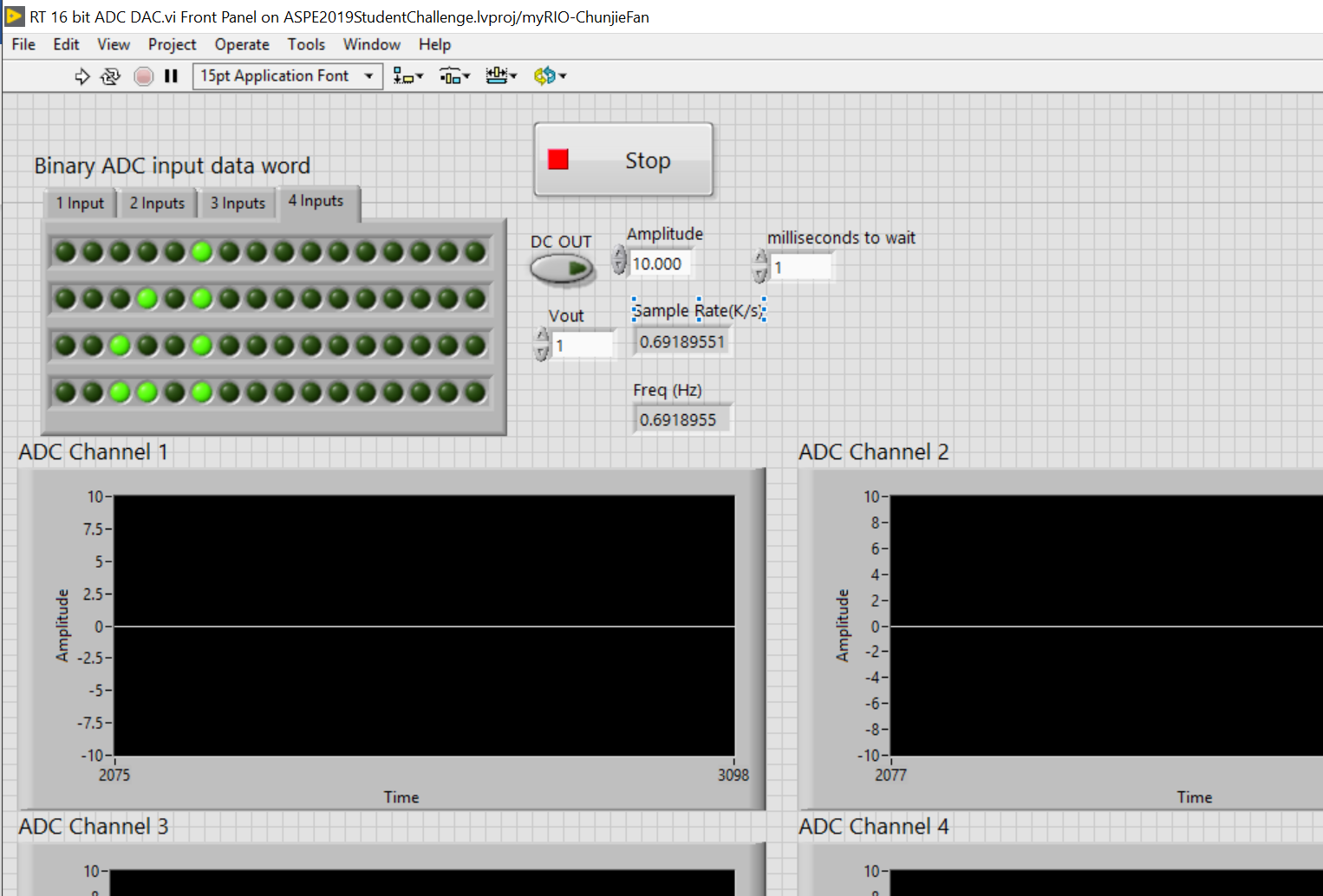


Figure : GUI for real-time amplifier monitoring and control.

The sample rate indicates the rate at which data is being collected.

Four options available with the tab selector provide the ability to read one, two, three, or four channels of the ADC. While the update rate of the DAC’s is not effected, because the ADC reads channels in series, reading multiple channels will slow the rate at which data is collected. An ADC read operation involves writing an input data word over the MOSI1 port followed by reading data from the MISO1 port.

The input data word this is sent to the ADC controls its operation. This is a 16 bit sequence with only the first 8 bits being used. The operation of these first eight bits is shown in Table 6 with a description in Table 7.

Table : Settings for the ADC input data word.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit # from left | SGL  DIFF | ODD | Select 1 | Select 0 | UNI | GAIN | NAP | SLEEP |
| Value | 0 | 0 | 1 or 0 | 1 or 0 | 1 or 0 | 1 or 0 | 0 | 0 |
| Comments | Differential  input | Polarity | Channel  Select 1 | Channel  Select 0 | Uni or bi-polar | Voltage range | Always 0 | Always 0 |

Table : Description of settings for the ADC input data word.

|  |  |  |
| --- | --- | --- |
| Bit | Name | Description |
| 1 | SGL  DIFF | Setting this bit determine whether or not the input is single ended (logic 1) or differential (logic 0).  Because the ADC is set up for differential this is always set to logic 0. |
| 2 | ODD | This enables switching polarity of the input pins.  Again this is configured for normal polarity and always set to logic 0. |
| 3 | Select 1 | The two select pins are used to determine the input channel to read. |
| 4 | Select 0 | Logic levels 0 0 reads channel 1, 0 1 reads channel 2, 1 0 reads channel 3, 1 1reads channel 4 |
| 5 | UNI | This enables switching between unipolar (logic level 1) and bipolar (logic level 0) inputs |
| 6 | GAIN | Two gain settings can be selected so that, depending on the setting of UNI, ranges of 0 - 5 V, ±5 V, 0 – 10 V, ±10 V can be set for any channel. |
| 7 | NAP | 0 power on. |
| 8 | SLEEP | 0 power on. |

1. Revision 1 8/25/2019 [↑](#footnote-ref-1)